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Design and Simulation of 16-bit Arithmetic Logic Unit using Memristor-based logic

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***Abstract*—**Current investigations into energy-efficient, high- speed nonvolatile memory devices with exceptional storage ca- pacity have captured the attention of researchers as they explore the emergence of a novel nanoscale solid-state ionic component, specifically the memristor, for upcoming advanced electronic systems.Memristortechnologystandsasahopefulconte nder to supplant traditional memory solutions, addressing significant designchallengesarisingfromthecontinuousreductioni ndevice dimensions. This paper centers on realizing a 16-bit Arithmetic Logic Unit through the utilization of memristors based on the Voltage Threshold Adaptive Memristor (VTEAM) model. The implementation involves coding in Verilog-A within the Cadence Virtuoso platform. The proposed design occupies notably less chip space than the conventional CMOS approach, while the decreased transistor count contributes to an enhancement in delay performance.

***Index Terms*—**Memristor, Arithmetic Logic Unit, Carry- lookahead Adder, Area, Delay

I. INTRODUCTION

The emergence of memristors, a class of nanoscale resis- tive switching devices, has sparked profound interest in the field of electronics and computation. Coined by combining ”memory”and”resistor,”thesedevicesshowcaseunique non- volatile memory properties and dynamic behavior, making them a promising avenue for advancing electronic systems. Memristors, first theorized by Leon Chua in 1971, offer the tantalizing prospect of memory and logic functions coexisting within a single component. This remarkable characteristic has led to the exploration of memristors as fundamental building blocksforneuromorphiccomputing,non-volatilememory,and novel computing paradigms.

Memristors captivate attention not just theoretically, but also due to their tangible real-world implications. Their small footprint, minimal energy usage, and seamless integrationinto traditional semiconductor manufacturing methods render them feasible contenders for incorporation into established electronic systems. Beyond this, memristors hold promise in tackling existing drawbacks of memory technology, such as the quest for elevated storage density and swifter data access. These exceptional attributes have sparked a wave of research endeavorsaimedatcomprehending,modeling,andharnessing the potential of memristors for a wide array of applications in computing and beyond.

The structure of this paper is as follows. In Section II, comprehensive insights into the design methodology are pre- sented. Section III delves into a thorough explanation of the intricate design and realization of the Arithmetic Logic Unit (ALU). Moving on to Section IV, an in-depth presentation of the simulation outcomes and their corresponding analysis is provided. Finally, the paper is concluded in Section V.

II. DESIGNMETHODOLOGY

The project’s design methodology encompasses a series of essentialphases,eachcontributingsignificantlytothecreation of an efficient Arithmetic Logic Unit (ALU) that operates on memristor-based logic principles. Initiating the process, the first stage involves the intricate modeling of the memristor device itself. This step revolves around crafting a meticulous mathematical model that accurately captures the nuanced behavior of the memristor. Leveraging the widely utilized Verilog-A modeling language, this phase utilizes iterative simulationsandadjustmentstofine-tunethememristormodel, aligning it closely with the real-world characteristics of the actual device.

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Subsequently, the methodology transitions to the develop- ment of basic logic gates by harnessing the memristor-based logic model. These foundational gates, including NOT, AND, OR, among others, are meticulously constructed through the Verilog-Amemristormodel.Thesegatesserveasfundamental building blocks that will later facilitate the creation of more intricate circuits. Following this, these foundational gates are ingeniously integrated to shape a comprehensive ALU circuit, capable of executing a wide range of arithmetic and logical operations. Upon the finalization of the ALU circuit's design, the third phase embarks on a rigorous simulation process. SpecializedtoolssuchasCadenceVirtuosoareemployed to subject the circuit to an array of diverse test scenarios, involving various input combinations for both arithmetic and logical computations. Through this simulation, the circuit's functionality,accuracy,andbehaviorundervaryingcond itions are meticulously evaluated. This crucial step aims to identify anypotentialinconsistenciesordeviations,leadingtoiter ative refinements of the circuit design.

Lastly, the project culminates in an in-depth analysis of the simulationoutcomes.Byscrutinizingcrucialperforman cemet- rics, including speed, power consumption, and accuracy, the strengths and limitations of the circuit become apparent. Fur- thermore, a comparative assessment might be conducted, con- trasting the memristor-based ALU with conventional CMOS- based counterparts. This thorough analysis unveils the advan- tages of adopting memristor-based logic, providing valuable insights into the circuit's overall efficacy and guiding any necessary optimization strategies.

III. DESIGNANDIMPLEMENTATION

A. ModellingI-Vcharacteristicsofmemristordevice

Modelling and realizing the I-V characteristics of a mem- ristor device is a fundamental aspect of understanding and harnessing the behavior of this innovative electronic com- ponent. Memristors, short for memory resistors, have gained immense attention in recent years due to their unique abilityto remember and alter their resistance based on the history of applied voltage and current. The I-V characteristics hysteresis curve is realized in the given below Figure 1.

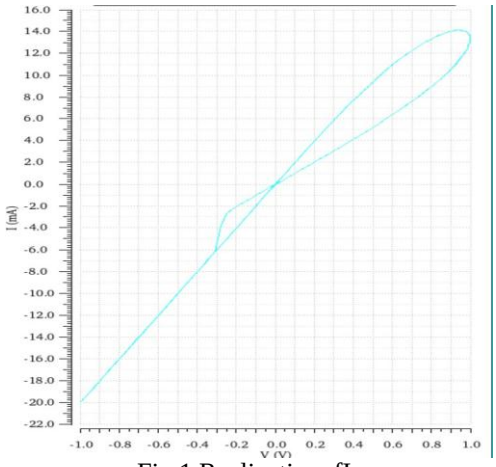

Fig.1.RealizationofI-Vcharacteristicsofamemristordevice

B. Designof8:1multiplexer

The 8:1 mux is used in this implementation for realizing eightfunctionswhichinvolvebotharithmeticandlogicop era- tions.Ithasthreeselectlinesforimplementingeightfuncti ons. The circuit of mux is shown in below Figure 2. The basic structure of an 8:1 mux consists of eight data inputs (D0 to D7), three control inputs (A, B, and C), and one output (Y). The three control inputs determine which of the eight data inputs is transmitted to the output.

Realization of eight functions are selected and listed in below table which indicates types of operations for cor- responding select lines of 3-bit length. Each 3-bit binary sequencehasallottedforoneparticularoperationasshow n in Figure 3.

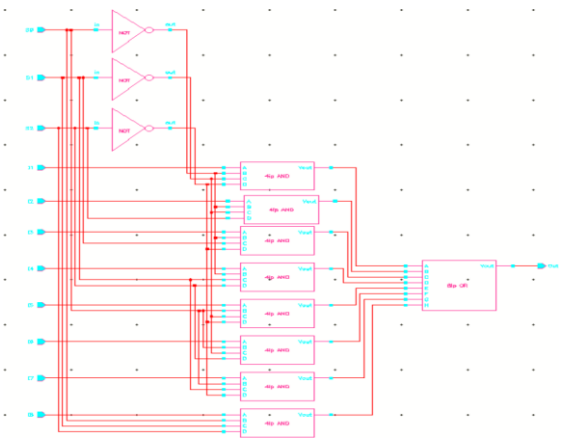

Fig.2.8:1multiplexercircuit

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Realization of eight functions are selected and listed in below table which indicates types of operations for cor- responding select lines of 3-bit length. Each 3-bit binary sequencehasallottedforoneparticularoperationasshow n in Table I.

TABLEI
TRUTHTABLEOFPROPOSEDARITHMETICLOGICUNIT

Operation	Selectionlines		
	S0	S1	S2
Addition	0	0	0
XOR	0	0	1
XNOR	0	1	0
NAND	0	1	1
Subtraction	1	0	0
AND	1	0	1
OR	1	1	0
XOR	1	1	1

C. Designof1-bitArithmeticLogicUnit

The Arithmetic Logic Unit (ALU) operates by receiving a pairof1-bitbinaryinputsdenotedasAandB,inaddition to control signals that specify the desired operation. Notably, memristors have the capacity to retain binary values. For instance,amemristorwithhighresistancecansignify0,w hile a memristor with low resistance can symbolize 1.1-bit ALU circuit is shown in the Figure 3.

The utilization of a carry-lookahead adder serves the pur- pose of addition due to its distinguished rapid operational nature. This design choice is rooted in its ability to circum- vent the delay associated with carry propagation that often hampers conventional ripple carry adders. The Carry Look- Ahead Adder effectively tackles this concern by concurrently computing carry signals for all bit positions, in contrast to the sequential approach of the ripple carry method. This substan-tialenhancementincalculationmethodremarkablyenha nces

the overall speed of addition. Comprising two primary com- ponents, namely the carry generator and the carry propagation blocks, the Carry Look-Ahead Adder efficiently addresses these challenges and ensures efficient addition operations.

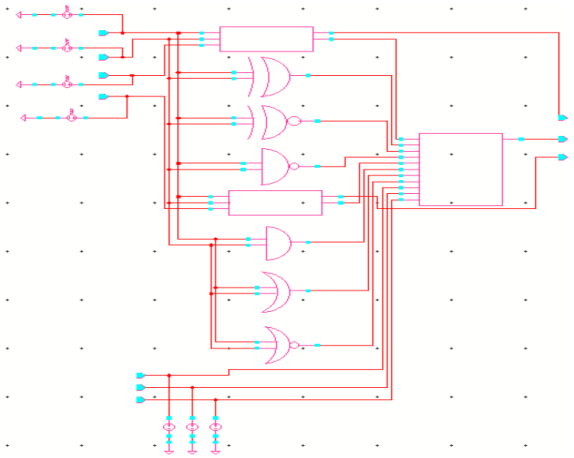

Fig.3.1-bitArithmeticLogicUnitcircuit

D. Designof16-bitArithmeticLogicUnit

The process of crafting a 16-bit Arithmetic Logic Unit (ALU)throughtheintegrationofmemristordevicesintan dem with transistors encompasses the development of a circuit capable of executing fundamental arithmetic and logic com- putations on a pair of binary inputs. The ALU is configuredto process two 16-bit binary inputs denoted as A and B, supplementedbycontrolsignalsS0,S1,S2,aswellasborr ow- in and carry-in bits that facilitate the selection of desired operations.AsaresultoftheseinputsandoperationstheA LU produces a 16-bit output in addition to carry-out and borrow- out bits, contributing to its comprehensive functionality.16-bit ALU circuit is shown in the Figure 4.

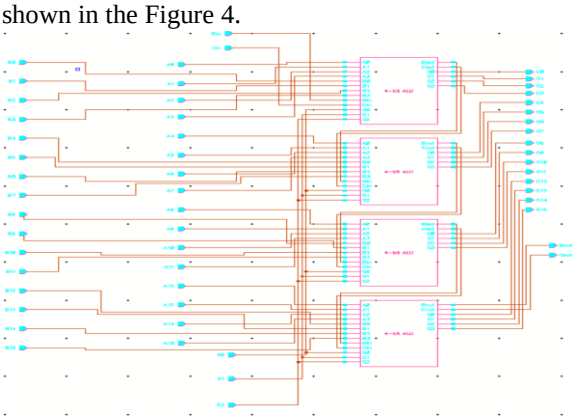

Fig.4.16-bitArithmeticLogicUnitcircuit

IV. RESULTS AND DISCUSSION

A. SimulationResult

Thesimulationanalysisofthefulladderfordifferentinput s iscarriedoutandtheresultsareobtainedascorrectlyassho

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wn in Figure 5.

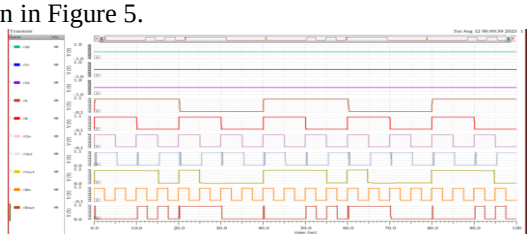

Fig.5.FulladderlogicsimulationanalysisinALU

Here A, B & Cin are the input data and Sum, Cout are the outputdata.Inputdataalsoinvolvestriggeringselectlines (S0, S1, S2) according to the truth table of ALU select lines forfull adder are set to S0=0, S1=0, S2=0 for obtaining full adder operation.

The simulation analysis of the full subtractor for different inputs is carried out and the results are obtained as correctlyas shown in Figure 6.

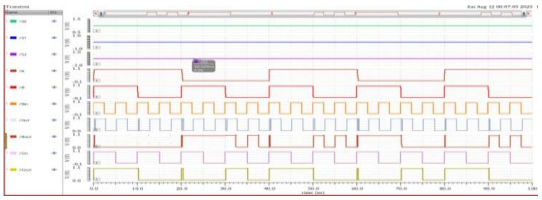

Fig.6.FullsubtractorlogicsimulationanalysisinALU

Here A, B & Bin are the input data and Difference, Boutare the output data. Input data also involves triggering select lines(S0, S1, S2) according to the truth table of ALU select lines for full subtractor are set to S0=1, S1=0, S2=0 for obtaining full subtractor operation.

The simulation analysis of the Arithmetic Logic Unit for different inputs is carried out and the results are obtained as correctly as shown in Figure 7.

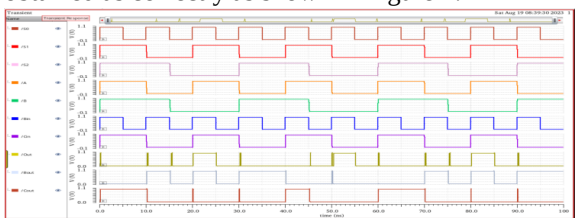

Fig.7.ArithmeticLogicUnitsimulationanalysis

Here A, B, Cin & Bin are the input data and Diff, Bout,Out, Sum, Cout are the output data. Input data also involves triggering select lines(S0, S1, S2) according to the truth table of ALU select lines are varied along transient period and corresponding outputs of the operations are obtained.

B. ComparativeAnalysis

Comparative results of using traditional CMOS and mem- ristor based circuit.

TABLEII

DEVICEUSAGECOMPARISONBETWEENTRADITIONALCMOS ANDMEMRISTOR BASED DESIGN

Unit	CMOS	Hybrid		
	Transistor	Memristor	Transistor	Total
AND	6	2	0	2
OR	6	2	3	2
8:1 mux	72	25	33	58
Full adder	42	10	10	20
1-bit ALU	176	44	62	106
16-bit ALU	2816	400	528	928

The proposed structure occupied much lesser die area with about67%improvementincomparisontoCMOSbased16-bit ALU as shown in Table II.

TABLEIII

DELAYCOMPARISONBETWEENTRADITIONALCMOS ANDMEMRISTORBASED DESIGN

Logic	CMOS	CMOS+Memristor	% improvement
Propagation delay (worst case)	0.8941 ns	0.6124 ns	32 %

The proposed structure improves delay by 32% as shownin Table III.

V. CONCLUSION

AmemristoremployingaVerilog-Abasedvoltagethreshold has been simulated and modeled. Through the use of the CadenceVirtuosotool,parametricanalysis,hysteresisplotting, aswellasarithmeticandlogicaloperationswereexecuted to showcase the effectiveness of the VTEAM model. The current study reveals that the read operation surpasses the write operation in terms of speed when compared to existing models.Consequently,thememristivemodelwassuccessfully integrated into the design of a 16-bit ALU. Impressively, the proposed configuration occupies significantly less die area, demonstrating a remarkable 67% enhancement in comparison to a CMOS-based 16-bit ALU design. Moreover, the decrease in transistor count contributes to a 32% reduction in delay, further optimizing the performance of the design."

REFERENCES

[1] P. Barla, V. K. Joshi, and S. Bhat, "A novel low power and reducedtransistorcountmagneticarithmeticlogi

cunitusinghybridstt-mtj/cmoscircuit," IEEE Access, vol. 8, pp. 6876–6889, 2020. doi: 10.1109/AC-CESS.2019.2963727.

[2] M. Nawaria, S. Kumar, M. K. Gautam, et al., "Memristor-inspireddigital logic circuits and comparison with 90-/180-nm cmos technologies," IEEE Transactions on Electron Devices, pp. 1–7, 2023. doi:10.1109/TED.2023.3278625.

[3] M. Zahedi, T. Shahroodi, S. Wong, and S. Hamdioui, "Efficient signedarithmetic multiplication on memristor-based crossbar," IEEE Access,vol.11,pp.33964–33978,2023.doi:10.1109/ACCESS.2023.3263259.

[4] A. Sasi, M. Ahmadi, and A. Ahmadi, "Low power memristor-basedshiftregisterdesign,"in202027thIEEEInternationalConferenceon Electronics, Circuits and Systems (ICECS), 2020, pp. 1–4. doi:10.1109/ICECS49266.2020.9294907.

[5] C.K.Jha,A.Mahzoon,andR.Drechsler,"Investigatingvar-iousadderarchitecturesfordigitalin-memorycomputingusingmagic-based memristor design style," in 2022 IEEE InternationalConference on Emerging Electronics (ICEE), 2022, pp. 1–4. doi:10.1109/ICEE56203.2022.10117915.

[6] K. Mbarek, F. O. Rziga, S. Ghedira, and K. Besbes, "Design andproperties of logic circuits based on memristor devices," in 2020 IEEEInternational Conference on Design Test of Integrated Micro Nano-Systems (DTS), 2020, pp. 1–5. doi: 10.1109/DTS48731.2020.9196059.

[7] F. Mozafari, M. Javad Sharifi, A. Ahmadi, and M. Ahmadi, "A novelarchitecture for memristor-based logic," in 2021 IEEE InternationalMidwest Symposium on Circuits and Systems (MWSCAS), 2021, pp.812–815. doi: 10.1109/MWSCAS47672. 2021.9531835.

[8] L.VinukolluandP.Kesari,"Areaefficientcarrylookaheadadderbasedon memristor ratioed logic," in 2021 2nd International Conference onCommunication,ComputingandIndustry4.0(C2I4),2021,pp.1–4.doi:10 . 1109 / C2I454156 . 2021.9689387

[9] Z. Chang, A. Cui, Z. Wang, and G. Qu, "Novel memristor-basednonvolatile d latch and flip-flop designs," in 2021 22nd InternationalSymposium on Quality Electronic Design (ISQED), 2021, pp. 244–250.doi: 10.1109/ISQED51717.2021.9424269.

[10] N. Kaushik and B. Srinivasu, "Implementation of imply-basedmemristivesubtractor,"in2022IEEE22ndInternationalCon-ference on Nanotechnology (NANO), 2022, pp. 523–526. doi:10.1109/NANO54668.2022.9928713.

[11] S. Kvatinsky, A. Kolodny, U. C. Weiser, and E. G. Friedman,"Memristor-basedimplylogicdesignprocedure,"in2011IEEE29thInternationalConferenceonComputerDesign(ICCD),2011,pp.142–147.doi: 10.1109/ICCD.2011.6081389.

[12] M.Teimoory,A.Amirsoleimani,A.Ahmadi,and M.Ahmadi,"Ahybridmemristorcmos multiplier design based on memristive universal logicgates,"in2017IEEE60thInternationalMidwestSymposiumonCircuitsandSystems(MWSCAS),2017,pp.1422–1425.doi:10.1109/MWSCAS.2017.8053199

[13] G. Zheng, S. P. Mohanty, E. Kougianos, and O. Okobiah, "Polynomialmetamodel integrated verilog-ams for memristor-based mixed-signalsystemdesign,"in2013IEEE56thInternationalMidwestSympo-sium on Circuits and Systems (MWSCAS), 2013, pp. 916–919. doi:10.1109/MWSCAS.2013.6674799.

[14] A.Chakraborty,A.Dhara,andH.Rahaman,"Designofmemristor-basedup-downcounterusingmaterialimplicationlogic,"in2016InternationalConferenceonAdvancesinComputing,CommunicationsandInformat-ics(ICACCI),2016,pp.269–274.doi:10.1109/ICACCI.2016.7732058.

[15] K.Mbarek,S.Ghedira,F.O.Rziga,andK.Besbes, "Designandanalysisof non-volatile memristor-based s-r latch," in 2020 IEEE InternationalConference on Design Test of Integrated Micro Nano-Systems (DTS),2020, pp. 1–5. doi: 10.1109/DTS48731.2020.9196039

[16] Q. Chen, X. Wang, H. Wan, and R. Yang, "A logic circuit design forperfectingmemristor-basedmaterialimplication,"IEEETransactionsonComputer-AidedDesignofIntegratedCircuitsandSystems, vol.36,no.2, pp. 279–284, 2017. doi: 10.1109/TCAD.2016.2578881.

[17] M. Elshamy, H. Mostafa, and M. S. Said, "Design considera-tions/insightsformemristor-basedmemoryarrays,"in2014InternationalConferenceonEngineeringandTechnology(ICET),2014,pp.1–6.doi:10.1109/ICEngTechnol.2014.7016789.