International Journal of Engineering, Management and Humanities (IJEMH)
Volume 5, Issue 6, Nov.-Dec, 2024 pp: 342-346ISSN: 2584-2145
www.ijemh.com

Improving Gain and Matching in 1 GHz LNAs; A Study on Simulation and Implementation

Laith M. Al Taan[1], Mohammed H. Shinen[2], Rana Z Al-Flayih[1], Haitham A. Ayoob[1]
[1]Department of Physics, College of Science, University of Mosul
[2]College of Science, University of Babylon

Date of Acceptance: 16-12-2024

Abstract

This study presents the design, simulation, and practical implementation of a low-noise amplifier (LNA) operating at 1 GHz using a FET transistor. The simulation results indicate an input reflection coefficient of (-10dB), an output reflection coefficient of (-19dB), and a forward gain of (12dB), demonstrating effective output matching and moderate input matching. Practical measurements show an amplified gain of (17dB), which exceeds the simulated values due to reduced parasitic effects and real-world material influences. The findings emphasize the importance of substrate selection in minimizing radiation losses and achieving optimal performance.

Keywords:LNA, gain, matching, simulation

I. Introduction

A Field-Effect Transistor (FET) biased Low-Noise Amplifier (LNA) operating in the frequency range of 800-1000 MHz is vital for modern communication systems, particularly in applications such as cellular networks, satellite communications, and wireless broadband. The primary function of an LNA is to amplify weak signals while adding minimal noise, thereby preserving signal integrity. FETs are commonly used as active devices in LNAs due to their high input impedance and low noise characteristics. The performance of an LNA, particularly its noise figure, gain, and linearity, is heavily influenced by the biasing conditions of the FET. Optimizing these conditions within the 800-1000 MHz frequency range is crucial for achieving high efficiency and reliability. Designing such LNAs requires careful consideration of factors such as power consumption, impedance matching, stability, and methods to minimize distortion and non-linearity. The use of FET types in the frequency range offers advantages in scalability and integration with RF systems so they are ideal candidates for the development of high-performance, low-noise amplifiers. (Rao*et al*., 2020; Zhang & Li, 2021; Huang *et al*., 2022). Recent advancements in materials, including advanced compound semiconductors and improved fabrication processes, have further enhanced the performance of LNAs designed for this frequency band (Yao andXu, 2023). The integration of modern design techniques and optimization algorithms, such as machine learning, is continually pushing the boundaries of LNA performance within this critical frequency range (Kim *et al.*, 2024). When designing low-noise amplifiers LNAs, careful study of bias conditions—particularly gate and drain voltages—is essential to ensure minimum noise figures and optimum performance.Ma *et al*., examined this topic in research papers (Ma *et al*, 2020), like which simplified small-signal models as well as constant noise characteristics which also rely heavily on mathematical derivations that provide limited intuitive design guidance. Feedback techniques, such as resistive and inductive methods, are frequently highlighted in publications like Singh *et al.* (2022), emphasizing their importance in enhancing gain and stability. Additionally, exploring power gates and dynamic voltage-frequency scaling to reduce power consumption is an emerging area of interest, as discussed in works such as Wang and Li (2023), particularly in the context of power-efficient LNA designs for battery-operated systems. The III-V compound semiconductors has a roll in enhancing LNA performance -especially regarding low noise and high efficiency, is well-documented in research, such as Huang *et al.* (2020). These materials are widely recognized for their advantages over traditional silicon, particularly in high-frequency and low-noise applications. Techniques for addressing non-linearity and intermodulation distortion are often discussed in LNA research. The feed-forward and feedback linearization methods are frequently referenced in studies like Zhang and Liu (2021). Finally, papers like Kim *et al.* (2024)

International Journal of Engineering, Management and Humanities (IJEMH)
Volume 5, Issue 6, Nov.-Dec, 2024 pp: 342-346ISSN: 2584-2145
www.ijemh.com

explore how some technologies can be leveraged to enhance the parameters and performance of RF components, including LNAs. In this work, a low-noise amplifier circuit will be designed for 1000MHz, using the Microwave Office MWO program. After simulating its performance, the lumped circuit will be manufactured using a FET transistor. Then, the appropriate dimensions for the distributed circuit elements will be calculated using the MATLAB program.

II. Method and Materials

2.1 Design Steps of a Low-Noise Amplifier (LNA)

The design of a Low-Noise Amplifier (LNA) consists of several steps. In this work the MWO software used where the design process begins with selecting the appropriate type of transistor and designing matching circuits for both the input and output Figure (1).Factors like the intended application, design type, and choice of substrate material, such as the ground plane, must be considered. The connection methods for components within the matching circuits are also determined. After the initial design, stability, and bias points are tested to verify performance. Transmission line dimensions are then calculated, often with the aid of computer-aided design (CAD) software for simulation and optimization.

2.2 Transistor Selection

The transistor is a fundamental component in low-noise amplifier (LNA) design, directly impacting critical parameters such as gain, bandwidth, and noise figure. The selection of an appropriate transistor type—typically MOSFET or FET—is crucial and depends on the application's requirements. FETs are widely chosen for high-frequency applications due to their high input impedance, low on-resistance, and minimal parasitic capacitance. These features enhance bandwidth and reduce power losses. Optimizing FET or MOSFET performance often involves biasing the device in its saturation region to achieve high transconductance while minimizing thermal noise. Which makes FETs particularly effective for wideband and high-frequency circuits.

In contrast, n-channel FETs are preferred in low-noise applications because of their higher electron mobility and reduced flicker noise, which result from the absence of an oxide interface in their channel. Multiparallel FET type configurations have been shown to further improve noise performance by reducing equivalent input-referred noise voltages and currents. This makes FETs suitable for sensitive analog systems where noise minimization is paramount (Yuqi*et al.,* 24). While MOSFETs provide higher gain and better scalability at higher frequencies, FETs excel in achieving ultra-low noise figures, particularly in circuits operating at lower frequencies or requiring extreme sensitivity. The choice of transistor type should, therefore, be guided by the specific performance priorities of the LNA design (Prasath*et al.,* 2020).

2.3 Substrate Selection

The substrate material plays a vital role in LNA design, affecting both circuit size and operational efficiency. A substrate with higher permittivity allows for smaller chip dimensions by reducing transmission line sizes and minimizing radiation losses. The effective permittivity must be calculated to ensure stable electric field distribution within the substrate, which is crucial for amplifier performance and stability. Selecting the right substrate is therefore critical for achieving efficient and stable LNA operation.

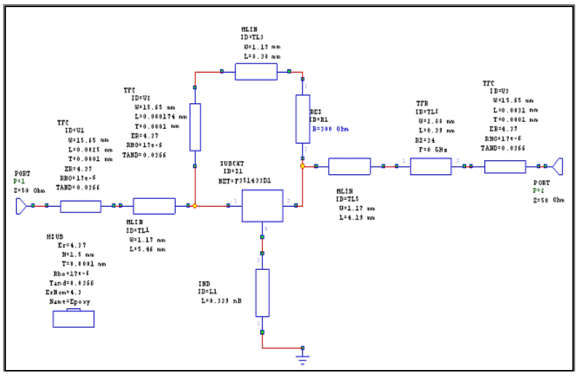
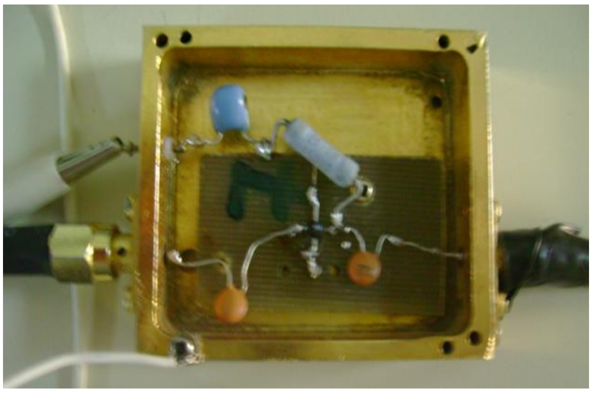


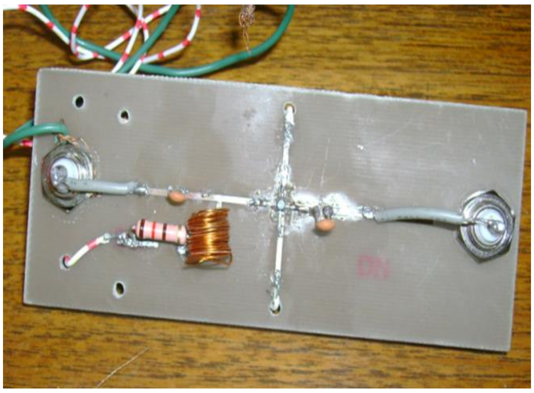
Figure 1: The simulation circuit for LNA

The LNA circuit, designed to operateat (1000 MHz), was fabricated on an epoxy substrate with a dielectric constant of (ε_r = 4.37), as shown in figure (2). The circuit was biased by applying a DC voltage of 10 volts. Subsequently, the signal was tested using a spectrum analyzer.

International Journal of Engineering, Management and Humanities (IJEMH)
Volume 5, Issue 6, Nov.-Dec, 2024 pp: 342-346ISSN: 2584-2145
www.ijemh.com



a



b

Figure 2: The LNA (a) the lumped circuit (b) distribution circuit

III. Results and Discussion

The simulation results of the lumped circuit using a transistor type (FET- F351433D1) were shown inFigure (3). The input S11 reflection coefficient, which was the lower value (-10dB) at 1 GHz. While the values of the output S22 reflection coefficient ranged from (-19dB) at 1GHz, which is a positive indication that the performance of the output matching circuit was better than the input.The forward gain coefficient S21 value was (12dB) at the working frequency (1GHz).

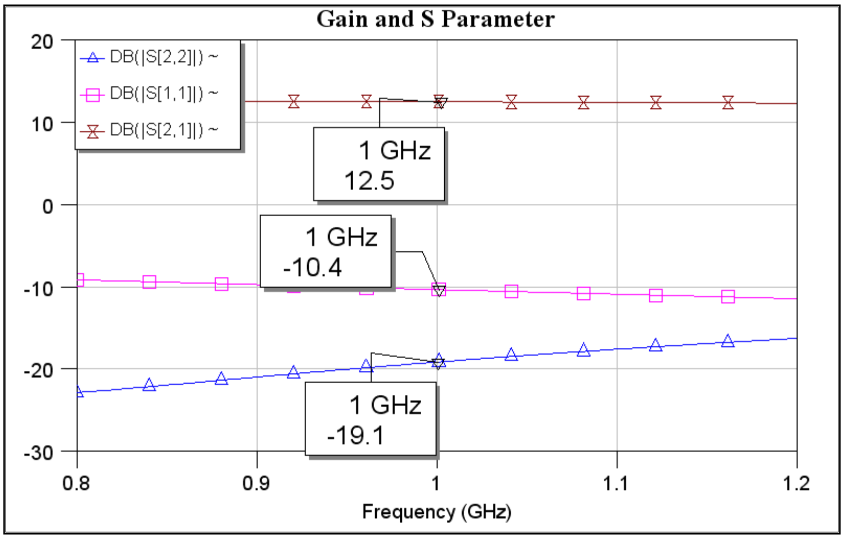
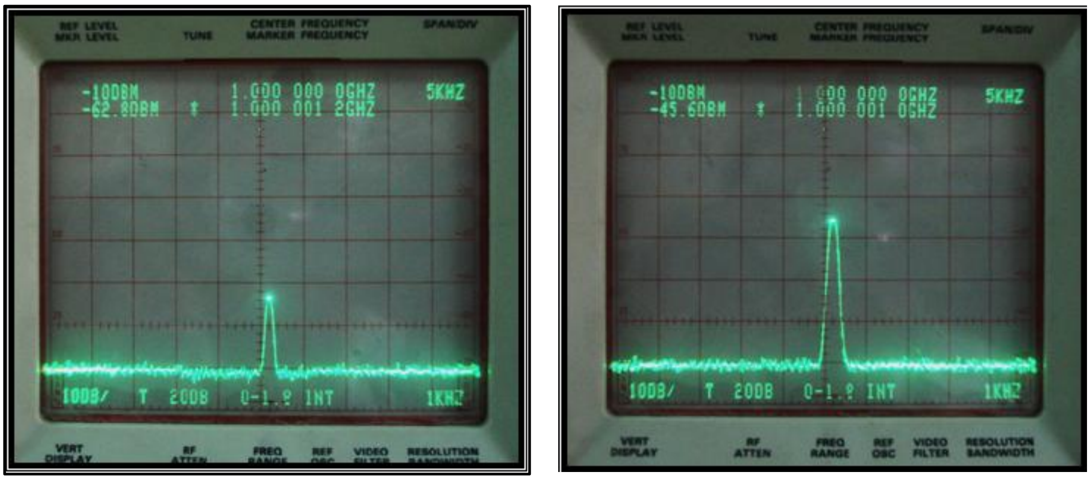


Figure (3): The S11, S22, and S21 coefficients of the FET lumped circuit at 1 GHz

Figure (4) shows the practical tests of the combined circuit at a frequency of 1 GHz, which were conducted using the frequency response, represented by the gain factor (G). This information was obtained with a spectrum analyzer. The signal level before entering the amplification stage was measured at (-62 dB), as shown in Figure (4-a) After passing through the circuit, the signal level rose to (-45 dB), as depicted in Figure (4-b). So the results indicate that the highest gain achieved at this frequency was (17 dB).



a b

Figure 4: The spectrum analyzer at 1 GHz shows the input signal (a), and output signal (b)

Using a suitable dielectric constant with this type (FET) may lead to better results, especially at such frequencies, and this is consistent with [Cardiol, 1988], as it reduces losses resulting from radiation.

Table (1): The simulation and practical results for the LNA circuit output using FET at 1GHz

Transistor	**Test**	**Gain (dB)**	**S_{11} (dB)**	**S_{22} (dB)**	**K(Stability)**	**Noise Figure (dB)**
ATF351433D	Simulation	12	-10	-19	1.04	1.58
ATF351433D	typically	17	-62	-45	-	-

From Table (1) it is also clear that the FET type transistor gave a higher gain value and a lower noise factor for the same frequency with close values in the reflection coefficients S22 and S11. As it is clear from above table, the practical results of FET type showed a higher gain value than the simulation**.**

IV. Conclusions

The analysis of both simulation and practical results demonstrates the effectiveness of the FET transistor in achieving significant amplification at 1 GHz. The simulated S11 and S22 values are -10 dB and -19 dB, respectively, which indicate moderate input matching and excellent output matching. However, further improvements in input matching could enhance the overall performance of the circuit. The practical gain observed was 17 dB, exceeding the simulated gain of 12 dB. This difference reflects the impact of real-world conditions, such as reduced parasitic and material properties. The findings highlight the importance of substrate selection; using appropriate dielectric constants can lead to performance improvements by minimizing radiation and substrate losses, as noted by Cardiol (1988). Additionally, the close alignment of practical and simulated reflection coefficients validates the reliability of the design and simulation process.

Future work should focus on refining the input matching network, exploring advanced dielectric materials, and optimizing transistor biasing to enhance gain and noise performance. These advancements would align with best practices outlined in RF design literature, including those by Pozar (2011) and other foundational studies.

Acknowledgment

The authors would like to thank the University of Mosul for its scientific support

References

[1] Cardiol, E. (1988). “RF Substrate Design Guidelines”. IEEE Transactions on Microwave Theory and Techniques.

[2] Cardiol, F.E, (1988), "Design and Layout of Microstrip Structures", IEEE proceeding, Vol.135, pt.H, No3 in Samir, Master Thesis. University of Mosul College of Science .

[3] Huang, Z., et al. (2020). “III-V compound semiconductors for high-performance low-

International Journal of Engineering, Management and Humanities (IJEMH)
Volume 5, Issue 6, Nov.-Dec, 2024 pp: 342-346ISSN: 2584-2145
www.ijemh.com

noise amplifiers". Journal of Applied Physics, 128(10), 154701.

[4] Huang, Z., Liu, J., & Chen, X. (2022). "Performance enhancement of FET-based LNAs in the 800-1000 MHz frequency band". IEEE Microwave and Wireless Components Letters, 32(1), 43–46.

[5] Kim, D., Choi, J., & Lee, S. (2024). "Artificial intelligence in the optimization of LNA design for low-noise and high-gain performance". IEEE Journal of Solid-State Circuits, 59(2), 256-265.

[6] Kim, D., Choi, M., & Lee, J. (2024). "Optimizing LNA design using artificial intelligence and machine learning". IEEE Journal of Solid-State Circuits, 59(1), 87-98.

[7] Ma, X., Zhang, H., & Li, L. (2021). "Noise figure optimization of low-noise amplifiers through biasing and feedback techniques". IEEE Transactions on Microwave Theory and Techniques, 69(12), 5121–5130.

[8] Pozar,D. M. (2011)."Microwave Engineering, 4th Edition". John Wiley& Sons.

[9] Prasath, C. S., Aruna T.(2020), "Design of Low Noise Amplifier using MOSFET Transistor for X-band Application", International Research Journal of Innovations in Engineering and Technology (IRJIET), Volume 4, Issue 2, pp 76-80.

[10] Rao, P., Sharma, A., & Gupta, V. (2020). "Low-noise amplifier design using FETs for wireless communication systems". IEEE Transactions on Microwave Theory and Techniques, 68(6), 1234–1243.

[11] Singh, R., & Kumar, P. (2022). "Improving LNA stability and gain through feedback networks". Journal of RF and Microwave Engineering, 47(4), 215–222.

[12] Wang, Y., & Li, S. (2023). "Low-power low-noise amplifier design: Power gating and dynamic scaling techniques". Journal of Semiconductor Electronics, 52(3), 1342–1351.

[13] Yao, S., &Xu, L. (2023). "Advances in compound semiconductor-based LNAs for RF communication applications". Journal of Semiconductor Technology and Science, 23(2), 134–141.

[14] Zhang, W., & Li, M. (2021). "Optimization of biasing techniques for low-noise amplifiers in the 800-1000 MHz range". Journal of RF and Microwave Engineering, 44(3), 158–165.

[15] Zhang, X., & Liu, F. (2021). "Mitigating non-linearity and intermodulation distortion in RF amplifiers". International Journal of RF and Microwave Computer-Aided Engineering, 31(5), e22807.

[16] Zhao,Y. , Tianyu Wang, Yang Zhang, Jun Lin.(2024): "Multi-parallel Differential JFET Low-Noise Amplifier Circuit Based on Discrete Current Source", IEEE Transactions on Instrumentation and Measurement, PP(99):1-1.doi: 10.1109/TIM.2024.3451602